Investigation on the Dynamic Characteristics of Hydrogen Passivated pGaN HEMTs Circuit Using ASM-GaN Model

Fan Li, Shiqiang Wu, Ang Li, Yuhao Zhu, Miao Cui, Jiangmin Gu, Ping Zhang, Yinchao Zhao, Huiqing Wen, Wen Liu

***Abstract*— This paper presents ASM-GaN model simulations of circuit-level analysis based on H_2 passivated pGaN/AlGaN/GaN HEMTs. The I-V characteristics of D-mode and E-mode HEMT devices are modeled, and subsequent research focuses on the impact of device capacitance on the dynamic properties of monolithic integrated circuits. The simulation results demonstrate that C_{ds}, C_{gd}, and C_{gs} have different effects on the logic circuit performances. The fitting of experimental data and simulation proves the credibility of the investigation of device capacitances. This work provides a direction to fit the dynamic output curve of the integrated circuit using the ASM-GaN model. The accurate fitting of the dynamic performance of Inverter, NAND, and Comparator circuits in this work will lay the foundation for the circuit design based on the GaN monolithic integration.**

***Index Terms*— ASM Model, DCFL circuit, Hydrogen Passivated GaN HEMTs, Capacitance, Dynamic Performance**

I. Introduction

In recent years, gallium nitride (GaN) has captured the attention of industry due to its superior properties, such as high operating temperature, high breakdown voltage, and fast switching speed [1]. Accurate device modeling is essential in integrated circuit design to mitigate errors that may arise from the fabrication process [2]–[4]. In GaN device simulation models, the Advanced Spice Model (ASM) has exhibited exceptional performance and has caught the interest of industries [5]–[8]. By leveraging various physical effect formulas [9], the ASM can represent the physical phenomena in GaN devices, including the trapping effect, velocity saturation effect, access region resistance effect, drain-induced barrier lowering (DIBL) effect, and temperature-dependent effect. Moreover, researchers have expanded the ASM applicability in various scenarios [7], [9], [10].

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Fan Li and Shiqiang Wu contributed equally to this work and should be considered co-first authors.

Fan Li, Shiqiang Wu, Ang Li, Yuhao Zhu, Miao Cui, Jiangmin Gu, Ping Zhang, Yinchao Zhao, Huiqing Wen, and Wen Liu are with the Department of Electrical and Electronic Engineering, Xi'an Jiaotong-Liverpool University, Suzhou 215123, China (e-mail: wen.liu@xjtlu.edu.cn).

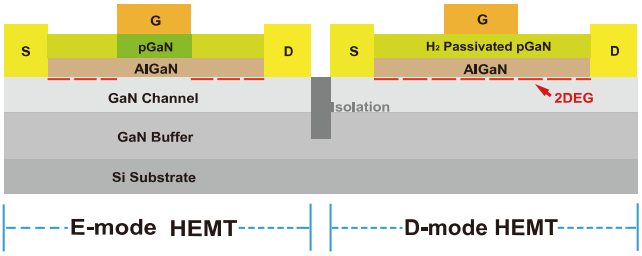

Fig. 1. H_2 passivated pGaN E/D-mode HEMT structures.

In the realm of GaN power electronics, the pGaN gate structure is a commercially available Enhancement-mode (E-mode) approach. However, during fabrication, the inductively coupled plasma (ICP) dry etching of the pGaN layer leads to etching damage, which reduces the devices' uniformity and stability. To address these reliability issues arising from surface states in pGaN HEMT, H_2 passivation presents a promising solution [11], [12]. For the GaN monolithic integration, early work on circuit simulation uses the GaAs model to characterize the HEMT devices [13], where the device model is not accurately fitted, so the circuit performance is unpredictable. Instead, the ASM-GaN model is preferred to provide accurate fittings. Although much ASM model-based progress has been done in radio frequency (RF) applications, The application of monolithic integrated circuits for power electronics is less common, especially for the components comprising monolithic mix-signal circuit modules.

This work utilizes the GaN-ASM model [14] to simulate H_2 passivated p-GaN HEMTs. The parameters are optimized to fit the static characteristics of the devices. Additionally, the model was used to simulate the monolithic integrated circuits. This analysis focused on establishing a connection between the device parameters and the dynamic performance of logic circuits so that the simulation can guide circuit design at a larger scale. Device capacitance data of power devices are referred from the datasheet because monolithic GaN HEMTs capacitance information is rarely reported. Finally, based on this analysis, the dynamic performance of the circuit was successfully fitted, facilitating subsequent design processes.

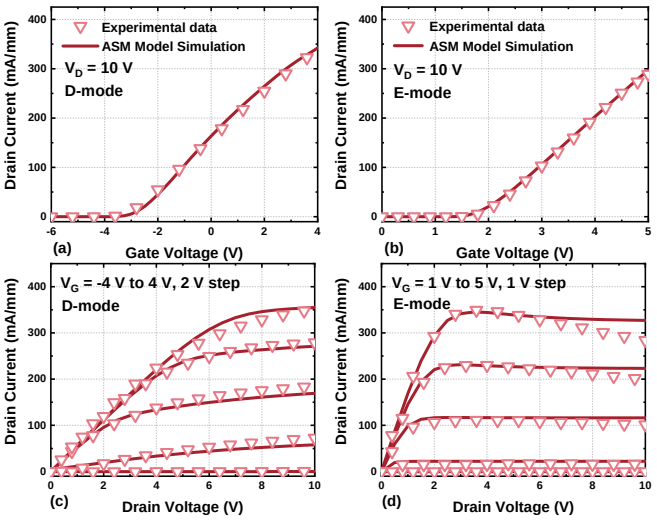

Fig. 2. Measured (dotted line) and simulated (solid line) device characteristics using ASM structure: transfer curves of (a) D-mode and (b) E-mode, output curves (c) and (d), $\boldsymbol{L_g/L_{gs}/L_{gd}/W_g}$= 2 μ m / 3 μm / 3 μm / 100 μm.

TABLE I
THE DEVICE CAPACITANCES RANGE OF PGAN HEMTS

References	C_{ds} (pF)	C_{gd} (pF)	C_{gs} (pF)
[16]	6.7	0.3	25.7
[17]	100	20	80
[18]	300	30	100
In this work	(30, 300)	(0.1, 30)	(25, 100)

II. THE SIMULATION OF THE H_2 PASSIVATED PGAN HEMTS DEVICE

The structure of the H_2 passivated pGaN E/D-mode HEMTs in this paper is shown in Figure 1, the ICP-induced H_2 plasma can form the Mg-H bond to passivate the pGaN layer so that the two-dimensional electron gas (2DEG) channel can be re-activated. The high-resistance H_2 passivated pGaN also serves as the dielectric layer for the D-mode HEMT. After importing the ASM-GaN model [14] into the Advanced Design System (ADS), the experimental data are used to extract the device parameters including VOFF, NFACTOR, CDSCD, ETA0, U0, NS0ACCS, VSATACCS, and RTH0 through the output and transfer characteristics. According to Ahsan et al., [15], these parameters significantly determine the intrinsic capacitances of HEMT devices. Then, these device parameters are added to the ADS. According to the simulation results shown in Figure 2, the transfer and output characteristics of D-mode and E-mode HEMTs were fitted. Figure 2 (a) presents the transfer curve of the D-mode HEMT, where the gate voltage was swept from -6 V to 4 V with the drain voltage at 10 V. Figure 2 (b) demonstrates the transfer curve of the E-mode HEMT with the gate voltage swept from 0 V to 5 V. The output curves of both HEMTs were displayed in Figure 2 (c) and Figure 2 (d).

After extracting the intrinsic capacitances of the device

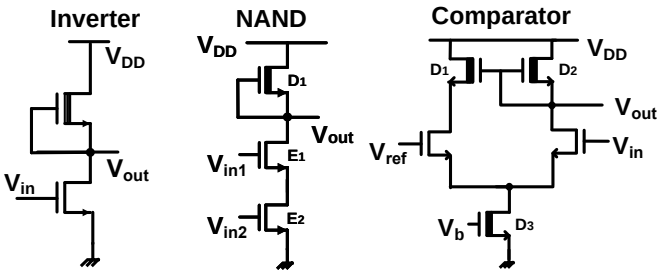

Fig. 3. Schematic of Direct-Coupled FET Logic (DCFL) inverter, NAND gate, and bootstrapped comparator circuit.

in DC sweep, the parasitic capacitances need to be found [15]. The parasitic capacitances are made up of access region capacitances, overlap capacitances, and fringing capacitances [14]. As the ASM manual instructed, the overlap capacitances (C_{dso}, C_{gso}, C_{gdo}) are used as one method to represent the realistic device capacitances (C_{ds}, C_{gd}, C_{gs}) in the following simulations. The industrial-level capacitance values were selected as the guidance for simulating the circuits, as illustrated in Table I. The values were chosen based on the report in [16] for C_{oss} = 7 pF, [17] for C_{ds} = 100 pF, and [18] for C_{ds} = 300 pF. The value of C_{gd} reported in [16] is 0.3 pF, while [10] suggests a value of about 6 to 9 pF, yet [17] and [18] indicates a 10 to 20 pF value. Consequently, the simulated device capacitance values are within the data range measured in the reference. The definitions between the input, output, and reverse capacitance and the device capacitance are illustrated in Equation 1.

$$\begin{aligned} Input\ Capacitance &: C_{iss} = C_{gd} + C_{gs} \\ Output\ Capacitance &: C_{oss} = C_{gd} + C_{ds} \\ Reverse\ Transfer\ Capacitance &: C_{rss} = C_{gd} \end{aligned} \quad (1)$$

The circuit diagrams in Figure 3 illustrate the Direct-Coupled FET Logic(DCFL) inverter, NAND gate, and bootstrapped comparator circuit in this study. For the following dynamic simulation of the DCFL inverter, a D-mode to E-mode gate width ratio of 30:100 was used; for the NAND circuits, a D-mode to E-mode gate width ratio of 10:200 was employed.

III. THE EXPLORATION OF DEVICE CAPACITANCES C_{ds}, C_{gd}, C_{gs} IN INVERTER CIRCUITS

This section demonstrates the impact of device capacitances on the dynamic performance of the inverter circuit. Equations 2-4 present the correlation of rise time τ_{rise}, fall time τ_{fall} with device parameters [19]. The voltage V_{DD} and $V_{T,D}$ ($V_{T,E}$) corresponds to the supply voltage and threshold voltage of D-mode HEMT (E-mode HEMT). In contrast, the $f\,(V_{DD}, V_{T,D})$ and $g\,(V_{DD}, V_{T,E})$ are independent to device capacitances variations. The μ_D and μ_E, $C_{ob,D}$ and $C_{ob,E}$ are mobility and gate barrier capacitances for D/E-HEMTs respectively. The load capacitance C_L is expanded in Equation 4 to link with device capacitances that are investigated in this section.

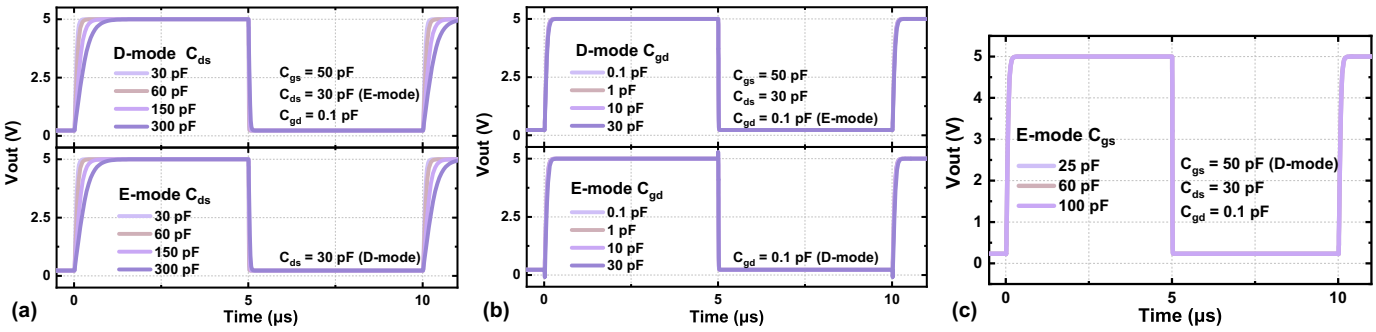

Fig. 4. (a) The simulated switching waveform (Frequency 100 kHz), setting (a) C_{ds}, (b) C_{gd} and (c) C_{gs} of E-mode and D-mode HEMTs as variables in inverter circuits.

$$\tau_{rise} = \frac{C_L}{\mu_D C_{ob,D}} \left(\frac{L}{W}\right)_D f\left(V_{DD}, V_{T,D}\right) \tag{2}$$

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ob,E}} \left(\frac{L}{W}\right)_E g\left(V_{DD}, V_{T,E}\right) \tag{3}$$

$$C_L = C_{gd,D} + C_{gd,E} + C_{ds,D} + C_{ds,E} + C_{int} \tag{4}$$

As depicted in Figure 4 (a), the performance of the inverter circuit in terms of C_{ds} has been investigated, revealing a degradation in the charging and discharging abilities as the C_{ds} of either the E-mode or D-mode HEMT increases. In the circuit, the D-mode HEMT could pull up the output voltage while the E-mode HEMT would pull down the output voltage. So, the significant difference between τ_{fall} and τ_{rise} can be attributed to the device gate width scale of D-mode: E-mode = 30:100. The gate width difference means a much stronger discharging current than the charging current. This explains why the τ_{fall} is much smaller than τ_{rise}. However, there is a difference in the impact of C_{ds} on the charging and discharging abilities. Specifically, if the capacitance C_{ds} is increased to the same extent for both HEMTs. The charging performance will be more severely affected compared with the discharging performance. In the inverter circuit, an increase in the C_{ds} value of either HEMT will weaken the charging and discharging capacities, as evidenced by the output voltage curve of the circuit.

In Figure 4 (b), it is demonstrated that C_{gd} has negligible impact on the charging and discharging capability of the inverter circuit. C_{gd} is known to have a relatively low value in GaN HEMTs [20]. C_{gd} has unnoticeable connections with the charging and discharging capability of the inverter circuit. In Figure 4 (c), the effect of C_{gs} on the charging and discharging ability of the inverter circuit is investigated. The simulation results indicate that increasing C_{gs} minimally impacts the performance of the inverter. The low capacitance value of C_{gs} has been reported by previous researchers [1], [9], [21].

IV. The Exploration of Device Capacitances C_{ds}, C_{gd}, C_{gs} in NAND Circuits

Figure 5 (a) depicts the input signals for the NAND circuits. The four phases result in four operating states, illustrated

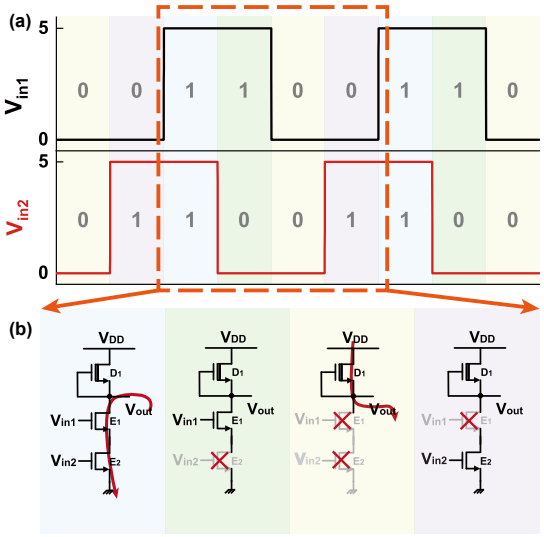

Fig. 5. The NAND setup (a) input signal (b) working stations of NAND circuits in 4 different phases.

in Figure 5 (b). Notably, each phase of input signals and operating conditions are depicted with the same color.

As illustrated in Figure 6 (a), increasing the C_{ds} of the D-mode HEMT in the NAND circuit from 30 pF to 300 pF noticeably amplifies the problem of unexpected voltage drops in the NAND output signal when it should remain logic high. Increasing the C_{ds} of the E-mode HEMT results in a higher voltage drop during the transition of the input signal (V_{in1} V_{in2}) from "00" to "01". This is because the E-mode HEMT has a path to the ground that can pull down the voltage level more effectively, causing the output voltage to drop significantly when a single E-mode HEMT is turned on. From the related work [8], [17], [18], three (C_{ds}) values have been reported. Therefore, based on the referenced data, these three C_{ds} values are selected for simulation. Firstly, the first two kinds of used simulated value C_{ds} = 30 pF, and C_{ds} = 90 pF are chosen to match the reported value in [8] and [17] separately. The last simulated value C_{ds} = 300 pF (150 pF for E-mode) capacitance is chosen to account for potential variations due to the fabrication process [18]. And the value of C_{gd} and C_{gs} selected in Figure 6 (b) and Figure 6 (c) are similar to the selection of C_{ds} in Figure 6 (a).

The investigation of C_{gd} in the NAND circuit has revealed

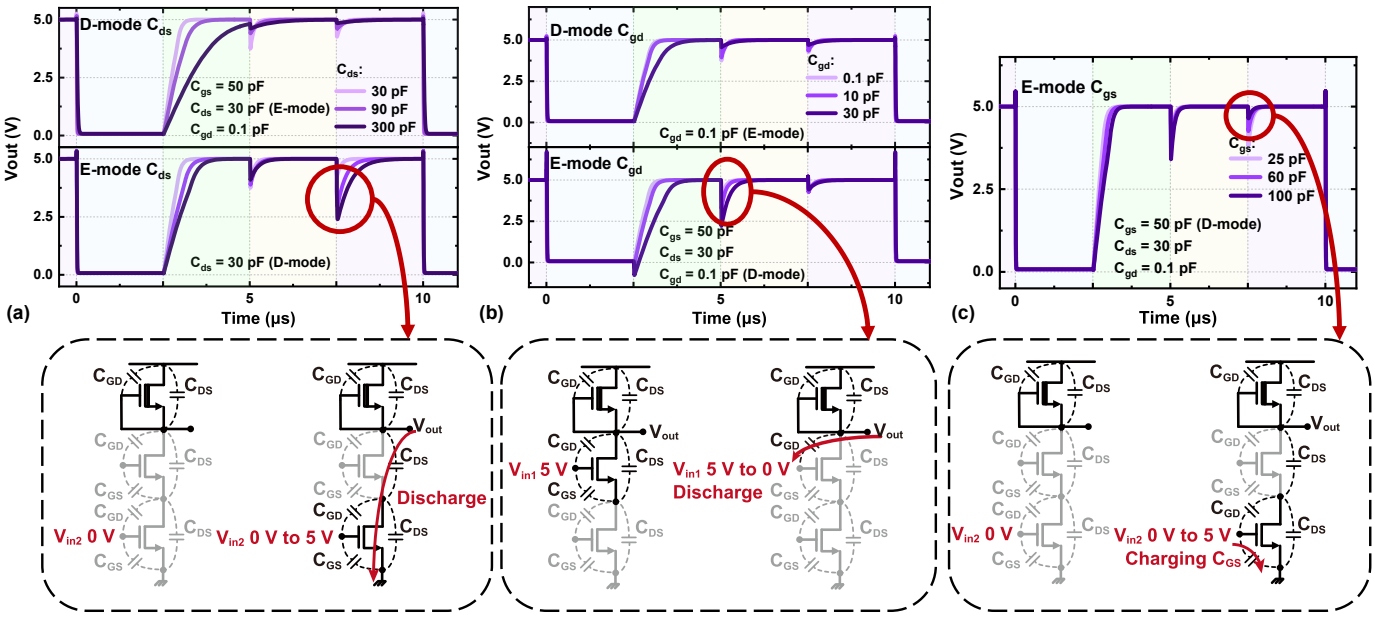

Fig. 6. (a) The simulated switching waveform (Frequency 100 kHz), setting (a) C_{ds}, (b) C_{gd} and (c) C_{gs} of E-mode and D-mode HEMTs as variables in NAND circuits.

two unique phenomena, as depicted in Figure 6 (b). Increasing the C_{gd} of the D-mode HEMT in the NAND circuit reduces the voltage drop of the output voltage when the input signal changes from "10" to "00". This is due to the increased ability of the D-mode HEMT to store charge, thereby enhancing the output voltage to maintain a high potential. Meanwhile, the voltage drop increases when the input voltage changes from "10" to "00", which is similar to the reason for increasing the E-mode C_{ds}. The voltage drop issue is considerably exacerbated by increasing the C_{gd} of the E-mode HEMT in the NAND circuit from 0.1 pF to 30 pF.

It has been observed that the C_{gs} of the E-mode HEMT affects the output of the NAND circuit, inferred from the data presented in Figure 6 (c). Increasing the C_{gs} of the E-mode from 25 pF to 100 pF leads to an increase in the voltage drop when "10" becomes "00". Simultaneously, an increase in voltage summits is observed when the input signal changes from "01" to "11". This can be attributed to the increase in charge stored in the E-mode HEMT due to the increase in C_{gs}, which releases more charge at the stage "11" input signal.

V. The Fitting Between the ASM Model Simulated Data and Experimental Result

After establishing the correlations between device capacitance and circuit performances in section III and section IV, it would be easier to exploit these conclusions to match the switching waveform of the three circuits in Figure 3. All the GaN H_2 passivated devices are also based on the platform proposed in that work [22]. Because all the experiments and simulations focus on the monolithic GaN HEMTs, the devices' capacitance in this section is meaningful for exploring the All-GaN HEMTs circuits.

The Figure 7 and Figure 8 correspond to the Inverter circuit. Specifically, Figure 7 depicts the inverter circuits' precise voltage transfer curve fitting, which captures the input voltage

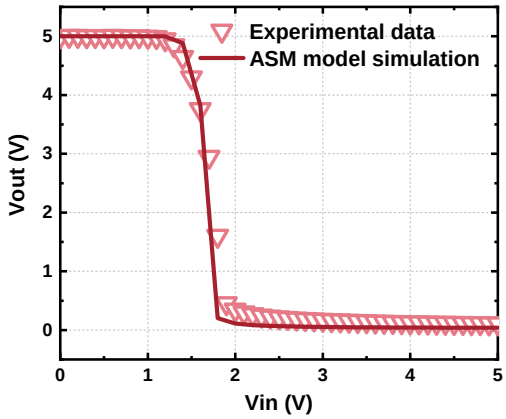

Fig. 7. The fitting of inverter circuit's voltage transfer curve between experiment data (scatter line) and ASM model simulation data (solid line).

range of 0 V to 5 V. The Inverter dynamic circuits are featured in Figure 8, with the upper figure representing the output at 100 kHz frequency and the lower figure corresponding to a frequency of 500 kHz. However, there are some voltage swings at the low output voltage. These ringing voltages are mainly caused by the parasitic inductive effect when V_{out} directly connecting to the ground. Figure 9 compares simulation and experimental results of NAND gate at a frequency of 100 kHz. The upper and lower figures correspond to different input phases. In Figure 10, the output response of the comparator circuit is fitted at different reference voltages from 2 V to 4 V, with a step voltage of 0.5 V.

From the inverter circuit, NAND circuit to the comparator circuit, even though the number of transistors in the circuit gradually increases. Although the simulation data still exhibits small deviations compared to the experimental data due to the nonideality in the real test environment setup, the results

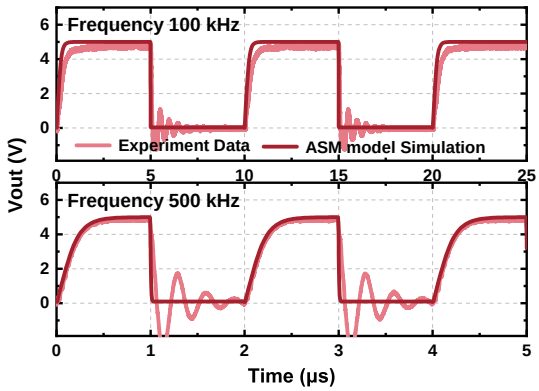

Fig. 8. The fittings of inverter's switching waveform between experiment data (light colored line) and ASM model simulation data (dark colored line) at 100 kHz and 500 kHz.

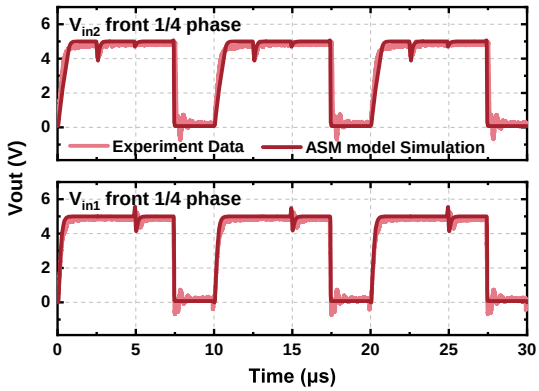

Fig. 9. The fitting of the NAND circuit's switching waveform between experiment data (light colored line) and ASM model simulation data (dark colored line) at 100 kHz, with two different phases.

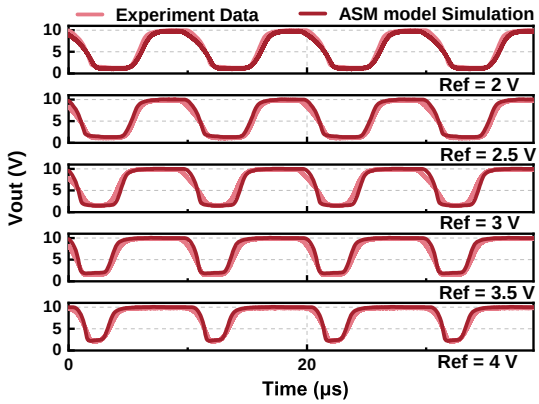

Fig. 10. The fitting of comparator circuit's switching waveform between experiment data (light colored line) and ASM model simulation data (dark colored line), within reference voltages equal to 2 V, 2.5 V, 3 V, 3.5 V, and 4 V.

still indicate that our approach of using device capacitance to model the dynamic characteristics of the circuit is reasonable and feasible.

VI. CONCLUSION

This paper applies the ASM-GaN model to fit the I-V curves of H_2 passivated pGaN gate HEMTs. We also identified potential issues that could arise in logic circuits composed of H_2 passivated devices through our exploration of the capacitance relationship. By investigating the device capacitances, we could accurately fit the dynamic characteristics of the Inverter, NAND, and comparator circuits. This process is beneficial to predict the monolithic GaN circuit switching performance and investigate the response rate of the device in each operating state relative to the dominant one of the three device capacitances (C_{gs}, C_{gd}, C_{ds}). This work provides a more intuitive understanding of the impact of device self-capacitance on the circuit and assures the feasibility of the IC platform design for H_2 passivated pGaN gate HEMTs.

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